IN THE SPECIFICATION

Please add the following paragraph beginning at page 8 line 12.

FIG. 7A is a plan view of first contact holes H in a second interlevel dielectric layer according to an embodiment of the present invention.

FIGS. 7B through 7D are cross-sectional views of the structure of FIG. 7A, taken along lines I-I', II-II', and III-III', respectively.

FIG. 8A shows a plan view of the structure stacked with bit line contact plugs, bit line structure, and storage node contact plugs according to an embodiment of the present invention.

FIGS. 8B through 8D are cross-sectional views of the structure of FIG. 8A, taken along lines I-I', II-II', and III-III', respectively.

FIG. 9A illustrates a plan arrangement of the capacitor lower electrode according to an embodiment of the present invention.

FIGS. 9B through 9D are cross-sectional views of the structure of FIG. 9A, taken along lines I-I', II-II', and III-III', respectively.